

CEDA PCB Design Review Process

PCB Design Checklist

This checklist is for the preparation of a PCB layout prior to the layout phase, during the layout and in the final layout review. There are many details that go into making a first-run board success.

The following elements of the PCB layout are covered:

1. Pad definition
2. Placement consideration
3. Routing guidelines and priorities
4. Testing considerations
5. Marking definitions and requirements
6. Fabrication

Pad definition

- Finished hole size is at least 10 mils larger than lead if no other data available
- Pads of through hole components are at least 12 mils larger than finished hole sizes
- Solder-mask does or does not cover via
- Solder paste openings are in proper size
- Tooling and mounting holes have internal plane clearance
- Thermal relief for internal power layers is defined
- Blind and buried via defined
- Ground test points sized for scope ground clip and easy access

Placement consideration

- Place through hole components on 50 mil grid
- Components and test pads are placed at least 200 mils from edge of board
- At least 15 mils spacing between components body
- Visible reference designators for automated assembly
- Component and trace void areas are observed
- Sufficient clearance for socket mounted ICs
- Clearances for IC extraction tools, emulator adapter and rework tools are considered
- There are standoffs for power resistors or other hot components
- Check the orientation of all connectors
- Bypass capacitors located close to IC power pins
- Place parts (especially ceramics) at least 50 mils (1.25 mm) from PCB edge
- Verify that all series terminators are located near the transmitter
- Verify that all parallel terminators are located near the receiver
- Place I/O drivers near the edge of the board where they leave
- High frequency crystal cases should be grounded
- No via under metal-film resistors and similar poorly insulated parts
- Try to populate the board evenly

Routing guidelines

- LVDS/differential/controlled impedance signals specified
- Digital and analog signal commons joined at only one point
- All nets have meaningful names with modifiers for signal polarity
- Ground planes where possible
- Traces are routed at least 20 mils (40 mils preferred) from edge of PCB
- Trace and space rules defined (5/5 is standard for signals)
- Trace width is sufficient for the current in the specific layer (Use IPC-2221 charts)
- Sufficient clearance for high voltage traces (Use IPC-2221 charts)
- Check for traces under noisy or sensitive components
 - Check that Power is not shorted to GND
- Provide multiple via (or one large via) for high current and/or low impedance traces
- Voltage regulator trace width are large enough for the output current desired

Testing considerations

- Test pad or test via on every net
- Test pads are evenly distributed (if possible) on one side of the PCB
- Test point on all unused outputs for debug use
- No logic pins connected directly to power or ground if in-circuit test is planned
- In circuit programming connectors are placed near the programmed device

Marking

- Silkscreen text fonts are larger than 36 mils (0.9 mm) wherever possible
- No silkscreen text over holes or pads
- All legend text reads in one or two directions
- If back annotate is required, prefer components labeled left-right, top-bottom
- All polarized components are marked for assembly orientation
- Company logo is in silkscreen layer
- Layers window is 'transparent' (free of solder mask or planes)
- PCB/Assembly part number on PCB (copper or silkscreen, top or bottom)
- PCB revision on silkscreen layer
- Assembly revision blank on silkscreen layer
- Serial number blank on silkscreen layer (top or bottom)
- All silkscreen text is readable when the board is populated
- All ICs have pin one clearly marked and visible when chip is assembled
- High pin count components have corner pins numbered for ease of location
- Silkscreen tick marks for every 10th or 20th pin on high pin count ICs and connectors

Fabrication

- Fabrication layer contains as a minimum:
 - PCB identification (part number and revision)
 - Date
 - Drill table shows all symbols and sizes
 - PCB specification
 - PCB thickness
 - Material
 - Copper weight on inner and outer layer
 - Finish
 - Editor identification
- Mounting holes matched 1:1 with mating parts
- Mounting holes electrically isolated or not
- Proper mounting hole clearance for hardware
- Tooling holes for automated assembly exist
- Tools on drill plot and NC drill file cross checked
- Solder mask over bare copper (SMOBC) noted if needed
- PCB thickness, material, copper weight and finish noted
- Solder mask and silkscreen type noted
- Photoplot/Gerber files checked using file viewer
- Panelized PCB fits assembly test and manufacturing equipment
- Ensure global board fiducials are present - minimum 3 per board in opposing corners
- In a panelized layout, ensure panel fiducials are present - 3 per panel in opposing corners

